UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS MARSHALL DIVISION

NETLIST, INC.

Plaintiff,

vs.

Civil Action No. 2:21-00463-JRG

JURY TRIAL DEMANDED

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.,

Defendants.

PLAINTIFF NETLIST INC.'S OBJECTIONS TO THE MAGISTRATE JUDGE'S MEMORANDUM OPINION AND ORDER REGARDING CLAIM CONSTRUCTION

Plaintiff ("Netlist") respectfully objects to Judge Payne's Memorandum Opinion and Order on claim construction dated December 14, 2022 (Dkt. 114) because certain constructions are clearly erroneous and contrary to law.

I. The '060/'160 Patent Family

"array die": Plaintiff respectfully objects to Judge Payne's construction of the term "array die" as "array die that is different from a DRAM circuit." Dkt. 114 at 31-32. Judge Payne construed the term based on alleged prosecution disclaimer. *Id.* But the prosecution statement and argument at issue is limited to Rajan's "DRAM circuits 206A-D," and not broadly to any DRAM circuits (as Samsung is apparently arguing):

First of all, Rajan does not disclose "a plurality of stacked array dies." Rajan merely stacks DRAM circuits 206A-D, which are different from array dies. As a result, Rajan's buffer chip 202 also operates very differently from the control die in claim 1. In rejecting claim 1, the Examiner states that Rajan (FIG. 2B) shows a memory package as recited in claim 1. The Examiner further cites Paragraph [0044] as disclosing the control die as recited in claim 1. Paragraph [0044] in Rajan, however, merely states:

Judge Payne stated at the hearing that it is up to the experts to explain and the jury to determine what "DRAM circuits" in the construction means. Ex. 1 at 33:15-34:11. But the construction as it is now phrased will cause confusion to the jury and does not accurately reflect what the inventor clearly and unmistakably stated during prosecution.

In Genuine Enabling Technology LLC v. Nintendo Co., Ltd., 29 F.4th 1365 (Fed. Cir. 2022), the Federal Circuit reversed the district court's claim construction and summary judgment. There, during prosecution, to distinguish prior art, the inventor argued that the prior art "taught 'slow-varying signals' whereas his inventions involved 'audio or higher frequency' signals" as input signals. Id. at 1374. The Federal Circuit observed:

The examiner's acceptance of that distinction and resulting decision to allow the claims suggest that [the inventor] and the examiner reached an understanding on that point. To the extent [the inventor's] statements may implicate other claim scope—such as signals of frequency up to 500 Hz—the record does not rise to the level of establishing a "clear and unmistakable" disavowal. *Tech. Props.*, 849 F.3d at 1358 (disclaimer is not established where statements are ambiguous or amenable to multiple reasonable interpretations).

Id. at 1374-75. As a result, the Federal Circuit rejected the district court's construction that the claimed "input signal" be limited to frequency of up to 500Hz. *Id.* at 1375 (The Federal Circuit observed: "Regarding the 500 Hz threshold, the district court erred by relying on expert testimony to limit the claim scope in a manner not contemplated by the intrinsic record.").

Here, like the intrinsic record in *Genuine* that did not support a finding of disclaimer of frequencies below 500Hz, the intrinsic record does not support a finding that the applicant distinguished anything but Rajan's specific "DRAM circuits 206A-D." *See Tech. Props. Ltd. LLC v. Huawei Techs. Co., Ltd.*, 849 F3d. 1349, 1359-60 (Fed. Cir. 2017) (revising the district court's construction because the patentee's prosecution statement only disclaimed *a particular use* of a command signal—using a command signal to change the clock frequency—but did not broadly disclaim an entire oscillator receiving a command input for any purpose). As a result, the Court should make clear that the claimed array die is one that is "different from Rajan's DRAM circuits 206A-D."

"chip select signal"/"chip select conduit": Judge Payne agreed with Samsung that "the plain and ordinary meaning of this term excludes situations in which a chip select signal could enable multiple array dies at once." Dkt. 114 at 33-34. It is unclear what Samsung (and Judge Payne) means by "enabl[ing] multiple array dies at once." To the extent that the Court means the chip select signal can only be driven to a single die, that is inconsistent with the specification. *Id.* at 34 (citing passages relating to driving a chip select signal to the array die corresponding to the chip

select signal and not to array dies that do not correspond to a chip select signal). For example, Figure 3 illustrates a conduit 332a having a driver 334a that is "configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b." '060 patent, 10:44-47. Likewise, conduit 332b having a driver 334b is "configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d." *Id.*, 10:47-50. The signals that may be driven along the die interconnects 334a and 334b include "a chip select signal." *Id.* 10:56-58, 10:62-67 (drivers 334 can be configured to drive signals other than data signals, such as chip select signals). Hence, in Figure 3, a chip select signal can be driven to both 310a and 310b along die interconnect 332a, and to both 310c and 310d along die interconnect 332b. Thus, to the extent that the construction is intended to limit the number of dies that the signal can be driven to, that is inconsistent with the specification.

Dated: December 28, 2022 Respectfully submitted,

By:/s/ Jason Sheasby

CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on December 28, 2022. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Jason Sheasby